AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for like-numbered paragraphs of the specification:

Please replace the paragraph on page 4, lines 13 – 22 with the following amended paragraph:

If the table is not prioritized correctly, then an incorrect route may be selected for the incoming packet. Figure 4 shows an example in which policy statement 201 is incorrectly prioritized such that it, rather than policy statement 203, is loaded into the lowest logical address. In this example, when policy search key 307 is provided to CAM array 304, priority encoder 306 still provides address zero on HPM bus 312. This causes, however, route information RI_0 to be selected in memory 308 rather than the desired route information RI_2 associated with higher priority policy statement ~~201~~ 203. It would be desirable to load policy statements into a CAM array without having to preorder the statements according to their respective priorities.

Please replace the paragraph on page 30, lines 5 – 23 with the following amended paragraph:

The timing of the compare circuit's 4603 operation is controlled through the use of an enable signal applied to enable input 4309 and the look-ahead enable signal (EI) received from a previous, or preceding in a row, compare circuit on enable input 4621. The enable signals EN and EI provide an enabling/disabling function to compare circuit 4603. The enable line (EN) 4309 is coupled to a first input of NAND gate 4611. A second input of NAND gate 4611 is coupled to receive ML segment $1210_{n-1,0}$. The output of NAND gate 4611 is coupled to a first input of NOR gate 4617. A second input of NOR gate 4617 is coupled to receive the D bit stored in memory element $1102_{n-1,0}$, and a third input of NOR gate 4617 is coupled to receive EI. In this manner, the enable signal is

NANDed with the signal on ML segment $1210_{n-1,0}$ such that transistor 4306 can turn on to discharge PNUM (depending on the logic state stored in memory element $1102_{n-1,0}$ and the logic state of match line segment $1210_{n-1,0}$) only if the enabling signals (e.g., a logic one in this circuit configuration) are asserted on enable lines 4309 and 4621. As will be appreciated by one skilled in the art, the operation of compare circuit ~~4303~~ 4603 may be represented logically as /PNUM = /EI AND (/D AND EN AND ML) and any logic or circuitry that implements this function may be used. Alternatively, compare circuit 4603 may have other logic configurations such that a logic zero may be an enabling signal.

Please replace the paragraph on page 30, lines 24 – 27, and page 31, lines 1-8, with the following amended paragraph:

The output (EO) of NOR gate 4619 is also coupled to the enable input signal (EI) of the next, or succeeding, compare circuit 4603_{n-2} in the row, as illustrated in Figure 45. The enable output signal (EO) is fed forward as the EI signal for the next compare circuit 4603_{n-2} in the row to enable the next compare circuit 4603_{n-2} without having to wait for transistors 1410 and 1412 in the current compare circuit 4603_{n-1} to resolve whether to deassert succeeding match line segment 4603_{n-2}. Such a feed-forward, look-ahead configuration allows for a next most significant priority line to be resolved concurrently with de-asserting succeeding match ~~lines~~ line segments in a ML row further reducing the amount of time required to resolve the match line segments and IADs. Any of transistors 4306, 1410, and 1412 can be replaced with other types of transistors and the logic adjusted accordingly.

Please replace the paragraph on page 31, lines 12 – 22 with the following amended paragraph:

Figure 47 is one embodiment of a compare circuit 4703 for the first column 1106_{n-1} of the priority table 4501 of Figure 45. The circuit configuration and operation of compare circuit 4703 is similar to that of compare circuit 4603 discussed above in relation to Figure 46, with the exception that (i) NAND gate 4611 also receives /D from memory element $1102_{n-1,0}$ and (ii) no enable input (EI) signal is applied to the circuit and, consequently, NOR gate 4617 of compare circuit 4603 is not needed and replaced with inverter 4717 in compare circuit 4703. NAND gate 4611 and inverter 4717 may [[[be]]]replaced with an AND gate. As will be appreciated by one of skill in the art, the operation of compare circuit 4703 may be represented logically as /PNUM = /D AND (EN AND ML) and any logic or circuitry that implements this function may be used.

Please replace the paragraph on page 68, lines 6 - 9 with the following amended paragraph:

The embodiment of Figure 35 can also insert and delete priority numbers assigned in descending priority order. Figure 38 shows such an example with of a 3x3 matrix in which row 0 stores priority number ~~111~~ 101 having the decimal equivalent of the number [[[~~7~~5]]], row 1 stores priority number ~~110~~ 111 having the decimal equivalent of the number 6, and row 2 stores priority number 101 having the decimal equivalent of the number [[[~~5~~7]]]. Thus, 111 is the most significant priority number, 110 is the next most significant priority number, and 101 is the least significant priority number.